Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for refreshing a memory system having a predetermined number of memory blocks, comprising:

providing a system refresh signal for refreshing the memory system, the system refresh signal being used as a first refresh request signal for refreshing a first memory block;

sequentially refreshing one or more subsequent memory blocks of the memory system while preventing more than one memory block from being ~~such that no two memory blocks are~~ refreshed at the same time,

wherein all the memory blocks are refreshed within a retention cycle of the memory system.

2. (Original) The method of claim 1 wherein the providing further includes generating the system refresh signal by a refresh timer coupled to the first memory block.

3. (Original) The method of claim 1 wherein the sequentially refreshing further includes sequentially generating one or more refresh request signals for the subsequent memory blocks.

4. (Original) The method of claim 3 wherein the sequentially refreshing further includes providing a refresh request signal by a refresh control circuit in each subsequent memory block to its immediately subsequent memory block while it is undergoing a refresh operation.

5. (Original) The method of claim 4 wherein the sequentially refreshing further includes generating a refresh command based on the refresh request signal for refreshing each memory block.

6. (Original) The method of claim 4 wherein the refresh commands for the memory blocks do not overlap in timing.

7. (Original) The method of claim 3 wherein the refresh requests do not overlap in timing.

8. (Currently amended) A memory system comprising:

a first memory block coupled to a refresh timer; and

one or more subsequent memory blocks without refresh timers contained therein,

wherein the refresh timer generates a system refresh signal for refreshing the memory system, and

wherein all memory blocks have a refresh controller contained therein which enables sequential refresh of the subsequent memory blocks while preventing more than one memory block from being ~~such that no two memory blocks are~~ refreshed at the same time.

9. (Previously presented) The memory system of claim 8 wherein the refresh controller of the first memory block receives the system refresh signal generated by the refresh timer.

10. (Original) The memory system of claim 8 wherein the refresh controller of each memory block generates a refresh request for an immediately subsequent memory block.

11. (Original) The memory system of claim 10 wherein the refresh controller of each memory block generates a refresh request for an immediately subsequent memory block when the memory block it belongs to is being refreshed.

12. (Previously presented) The memory system of claim 10 wherein the refresh requests generated do not overlap in timing.

13. (Previously presented) The memory system of claim 10 wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to.

14. (Previously presented) The memory system of claim 13 wherein the refresh commands generated do not overlap in timing.

15. The memory system of claim 8 wherein the refresh controller provides a refresh address.

16. (Currently amended) A dynamic random access memory system comprising:

a first memory block coupled to a refresh timer; and

one or more subsequent memory blocks without refresh timers contained therein,

wherein the refresh timer generates a system refresh signal for refreshing the memory system, and

wherein all memory blocks have a refresh controller contained therein which enables sequential refresh of the subsequent memory blocks, while preventing more than one memory block from being ~~such that no two memory blocks are~~ refreshed at the same time.

17. (Previously presented) The memory system of claim 16 wherein the refresh controller of the first memory block receives the system refresh signal generated

by the refresh timer.

18. (Previously presented) The memory system of claim 16 wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to and a refresh request for an immediately subsequent memory block when the memory block it belongs to is being refreshed.

19. (Previously presented) The memory system of claim 18 wherein the refresh requests generated do not overlap in timing.

20. (Previously presented) The memory system of claim 18 wherein the refresh commands generated do not overlap in timing.

21. (Previously presented) The memory system of claim 16 wherein the refresh controller provides a refresh address.